CLAIMS

What is claimed is:

1. A method for conversing battery power for a battery-optimized system-on-a-chip, the method comprises:

sensing for presence of an alternate power source;

when the presence of the alternate power source is detected:

disabling a first control loop of a first DC-to-DC converter, wherein, when enabled, the first DC-to-DC converter converts battery voltage from a battery into a supply voltage; and

enabling a second control loop of a second DC-to-DC converter, wherein the second DC-to-DC converter converts voltage from the alternate power source into the supply voltage.

2. The method of claim 1 further comprises:

when the presence of the alternate power source is not detected:

maintaining enablement of the first control loop; and

maintaining disablement of the second control loop.

3. The method of claim 1, wherein the enabling the second control loop further comprises:

adjusting voltage regulation sensing for the second DC-to-DC converter from a disabled voltage regulation sensing level to an active voltage regulation sensing level to produce an active regulation voltage;

comparing a reference voltage with the active regulation voltage to produce a regulation signal; and

providing the regulation signal to a linear regulator that is sourced via the alternate power source to produce the supply voltage, wherein linear regulator functions as the second DC-to-DC converter.

4. The method of claim 3 further comprises:

disabling the second control loop by adjusting the voltage regulation sensing for the second DC-to-DC converter from the active voltage regulation sensing level to the disabled voltage regulation sensing level to produce a disabled regulation voltage.

5. The method of claim 1, wherein the disabling the first control loop further comprises:

logically disabling a sink transistor of the first DC-to-DC converter; and

logically disabling a load transistor of the first DC-to-DC converter.

6. The method of claim 1 further comprises:

when the first control loop is disabled:

monitoring, by the first control loop, the supply voltage produced by the second DC-to-DC converter; and

when the supply voltage reaches a near steady-state condition, generating, by the first control loop, a valid supply voltage indication.

7. The method of claim 1, wherein the detecting the presence of alternate power source further comprises:

comparing the supply voltage to a voltage on a node operably coupled to the alternate power source; and

when the supply voltage compares unfavorably to the voltage on the node, determining that the alternate power source is present.

8. An optimized battery usage circuit for a comprehensive system-on-a-chip, the optimized battery usage circuit comprises:

a first DC-to-DC converter operable to convert a battery voltage into a supply voltage when an alternate power source is not coupled to the comprehensive system-on-a-chip; and

a second DC-to-DC converter operable to convert an alternate power source voltage into the supply voltage when the alternate power source is coupled to the comprehensive system-on-a-chip.

9. The optimized battery usage circuit of claim 8 further comprises:

alternate power source sense circuit operably coupled to determine whether the alternate power source is coupled to the comprehensive system-on-a-chip and to provide an alternate power source signal when the alternate power source is coupled to the comprehensive system-on-a-chip, wherein, when the alternate power source signal indicates the presences of the alternate power source, a control loop of the first DC-to-DC converter is disabled and a control loop of the second DC-to-DC converter is enabled and, when the alternate power source signal indicates that the alternate power source is not present, the control loop of the first DC-to-DC converter is enabled and the control loop of the second DC-to-DC converter is disabled.

10. The optimized battery usage circuit of claim 9 further comprises:

a multiple stage voltage divider operably coupled to provide an active regulation voltage and a disabled regulation voltage from the supply voltage, wherein the active regulation voltage is provided to the control loop of the second DC-to-DC converter when the alternate power source is present and the disabled regulation voltage is provided to the control loop of the second DC-to-DC converter when the alternate power source is not present.

11. The optimized battery usage circuit of claim 10 further comprises:

the first DC-to-DC converter including at least one of a buck topology and a boost topology; and

the second DC-to-DC converter including a linear regulator.

12. The optimized battery usage circuit of claim 11, where the first DC-to-DC converter further comprises:

a sink transistor operably coupled to an external inductor;

a load transistor operably coupled to the external inductor and the supply voltage; and

control loop module operably coupled to receive the active regulation voltage and, when the alternate power source is not present, to produce a sink drive signal and a load drive signal to drive, respectively, the sink transistor and the load transistor to produce the supply voltage and, when the alternate power source is present, the control loop module generates the sink and load drive signals to disable the sink and load transistors, respectively.

13. The optimized battery usage circuit of claim 11, where the control loop module further functions to generate a valid supply voltage when the alternate power source is present.

14. The optimized battery usage circuit of claim 10, where the control loop of the second DC-to-DC converter further comprises:

a multiplexer operably coupled to output the active regulator voltage or the disabled regulation voltage based on the alternate power source signal; and

an amplifier operably coupled to compare the output of the multiplexer with a reference voltage, wherein, when the output of the multiplexer is the active regulation voltage, the amplifier outputs a valid regulation signal such that the second DC-to-DC converter produces the supply voltage and, when the output of the multiplexer is the disabled regulation voltage, the amplifier outputs a regulation signal that disables the second DC-to-DC converter.

15. The optimized battery usage circuit of claim 9, wherein the alternate power source sense circuit further functions to:

compare the supply voltage to a voltage on a node operably coupled to the alternate power source; and

when the supply voltage compares unfavorably to the voltage on the node, generate the alternate power source signal to indicate that the alternate power source is present.

16. An apparatus for conversing battery power for a battery-optimized system-on-a-chip, the apparatus comprises:

a processing module operably coupled to:

sense for presence of an alternate power source;

when the presence of the alternate power source is detected:

disable a first control loop of a first DC-to-DC converter, wherein, when enabled, the first DC-to-DC converter converts battery voltage from a battery into a supply voltage; and

enable a second control loop of a second DC-to-DC converter, wherein the second DC-to-DC converter converts voltage from the alternate power source into the supply voltage.

17. The apparatus of claim 16, wherein the processing module further functions to:

when the presence of the alternate power source is not detected:

maintain enablement of the first control loop; and

maintain disablement of the second control loop.

18. The apparatus of claim 16, wherein the processing module further functions to enable the second control loop by:

adjusting voltage regulation sensing for the second DC-to-DC converter from a disabled voltage regulation sensing level to an active voltage regulation sensing level to produce an active regulation voltage;

comparing a reference voltage with the active regulation voltage to produce a regulation signal; and

providing the regulation signal to a linear regulator that is sourced via the alternate power source to produce the supply voltage, wherein linear regulator functions as the second DC-to-DC converter.

19. The apparatus of claim 18, wherein the processing module further functions to:

disable the second control loop by adjusting the voltage regulation sensing for the second DC-to-DC converter from the active voltage regulation sensing level to the disabled voltage regulation sensing level to produce a disabled regulation voltage.

20. The apparatus of claim 16, wherein the processing module further functions to disable the first control loop by:

logically disabling a sink transistor of the first DC-to-DC converter; and

logically disabling a load transistor of the first DC-to-DC converter.

21. The apparatus of claim 16, wherein the processing module further functions to:

when the first control loop is disabled:

enable monitoring, by the first control loop, the supply voltage produced by the second DC-to-DC converter; and

when the supply voltage reaches a near steady-state condition, generate, by the first control loop, a valid supply voltage indication.

22. The apparatus of claim 16, wherein the processing module further functions to detect the presence of alternate power source by:

comparing the supply voltage to a voltage on a node operably coupled to the alternate power source; and

when the supply voltage compares unfavorably to the voltage on the node, determining that the alternate power source is present.

23. A battery-optimized system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals;

a first DC-to-DC converter operable to convert a battery voltage into a supply voltage when an alternate power source is not coupled to the comprehensive system-on-a-chip; and

a second DC-to-DC converter operable to convert an alternate power source voltage into the supply voltage when the alternate power source is coupled to the comprehensive system-on-a-chip, wherein the supply voltage is provided to at least one of the processing core, the digital interface, and the mixed signal circuitry.

24. The battery-optimized system-on-a-chip of claim 23 further comprises:

alternate power source sense circuit operably coupled to determine whether the alternate power source is coupled to the comprehensive system-on-a-chip and to provide an alternate power source signal when the alternate power source is coupled to the comprehensive system-on-a-chip, wherein, when the alternate power source signal indicates the presences of the alternate power source, a control loop of the first DC-to-DC converter is disabled and a control loop of the second DC-to-DC converter is enabled and, when the alternate power source signal indicates that the alternate power source is not present, the control loop of the first DC-to-DC converter is enabled and the control loop of the second DC-to-DC converter is disabled.

25. The battery-optimized system-on-a-chip of claim 24 further comprises:

a multiple stage voltage divider operably coupled to provide an active regulation voltage and a disabled regulation voltage from the supply voltage, wherein the active regulation voltage is provided to the control loop of the second DC-to-DC converter when the alternate power source is present and the disabled regulation voltage is provided to the control loop of the second DC-to-DC converter when the alternate power source is not present.

26. The battery-optimized system-on-a-chip of claim 25 further comprises:

the first DC-to-DC converter including at least one of a buck topology and a boost topology; and

the second DC-to-DC converter including a linear regulator.

27. The battery-optimized system-on-a-chip of claim 25, where the first DC-to-DC converter further comprises:

a sink transistor operably coupled to an external inductor;

a load transistor operably coupled to the external inductor and the supply voltage; and

control loop module operably coupled to receive the active regulation voltage and, when the alternate power source is not present, to produce a sink drive signal and a load drive signal to drive, respectively, the sink transistor and the load transistor to produce the supply voltage and, when the alternate power source is present, the control loop module generates the sink and load drive signals to disable the sink and load transistors, respectively.

28. The battery-optimized system-on-a-chip of claim 27, where the control loop module further functions to generate a valid supply voltage when the alternate power source is present.

29. The battery-optimized system-on-a-chip of claim 24, where the control loop of the second DC-to-DC converter further comprises:

a multiplexer operably coupled to output the active regulator voltage or the disabled regulation voltage based on the alternate power source signal; and

an amplifier operably coupled to compare the output of the multiplexer with a reference voltage, wherein, when the output of the multiplexer is the active regulation voltage, the amplifier outputs a valid regulation signal such that the second DC-to-DC converter produces the supply voltage and, when the output of the multiplexer is the disabled regulation voltage, the amplifier outputs a regulation signal that disables the second DC-to-DC converter.

30. The battery-optimized system-on-a-chip of claim 24, wherein the alternate power source sense circuit further functions to:

compare the supply voltage to a voltage on a node operably coupled to the alternate power source; and

when the supply voltage compares unfavorably to the voltage on the node, generate the alternate power source signal to indicate that the alternate power source is present.

31. A battery-optimized system-on-a-chip comprises:

a processing core operably coupled to process input digital data and produce therefrom output digital data;

digital interface circuitry operably coupled to provide the input digital data to the processing core and to receive the output digital data from the processing core;

mixed signal circuitry operably coupled to convert input analog signals into the input digital data and to convert the output digital data into output analog signals;

a first DC-to-DC converter, when enabled, operable to convert a battery voltage into a supply voltage; and

a second DC-to-DC converter, when enabled, operable to convert an alternate power source voltage into the supply voltage, wherein the supply voltage is provided to at least one of the processing core, the digital interface, and the mixed signal circuitry, and wherein the processing core functions to:

sense for presence of the alternate power source;

when the presence of the alternate power source is detected:

disable a first control loop of the first DC-to-DC converter; and

enable a second control loop of a second DC-to-DC converter.

32. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to:

when the presence of the alternate power source is not detected:

maintain enablement of the first control loop; and

maintain disablement of the second control loop.

33. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to enable the second control loop by:

adjusting voltage regulation sensing for the second DC-to-DC converter from a disabled voltage regulation sensing level to an active voltage regulation sensing level to produce an active regulation voltage;

comparing a reference voltage with the active regulation voltage to produce a regulation signal; and

providing the regulation signal to a linear regulator that is sourced via the alternate power source to produce the supply voltage, wherein linear regulator functions as the second DC-to-DC converter.

34. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to:

disable the second control loop by adjusting the voltage regulation sensing for the second DC-to-DC converter from the active voltage regulation sensing level to the disabled voltage regulation sensing level to produce a disabled regulation voltage.

35. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to disable the first control loop by:

logically disabling a sink transistor of the first DC-to-DC converter; and

logically disabling a source transistor of the first DC-to-DC converter.

36. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to:

when the first control loop is disabled:

enable monitoring, by the first control loop, the supply voltage produced by the second DC-to-DC converter; and

when the supply voltage reaches a near steady-state condition, generate, by the first control loop, a valid supply voltage indication.

37. The battery-optimized system-on-a-chip of claim 31, wherein the processing core further functions to detect the presence of alternate power source by:

comparing the supply voltage to a voltage on a node operably coupled to the alternate power source; and

when the supply voltage compares unfavorably to the voltage on the node, determining that the alternate power source is present.